Electronic Version
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Claims

[c1] 1. A method of fabricating a thin film transistor array substrate, comprising:
forming a plurality of gates and a plurality of scan lines electrically connected to the gates on a substrate;
forming a gate insulating layer covering the gates and the scan lines;
forming a channel layer and an ohmic contact layer on the gate insulating layer above the gates;
forming a transparent conductive layer over the substrate;
forming a metal layer on the transparent conductive layer;
patterning the metal layer and the transparent conductive layer to form a plurality of source/drain regions, a plurality of data lines and a plurality of pixel regions;
forming a passivation layer over the substrate exposing the metal layers on the pixel regions; and
removing the metal layer exposed by the passivation layer to expose the transparent conductive layer on the pixel regions, using the passivation layer as a mask, wherein the transparent conductive layer on the pixel regions serves as a plurality of pixel electrodes.

[c2] 2. The method of fabricating the thin film transistor array substrate of claim 1, further comprising forming a plurality of first transparent conductive layers on the gates and the scan lines.

[c3] 3. The method of fabricating the thin film transistor array substrate of claim 1, wherein the step of forming the gates and the scan lines further comprises forming a plurality of first terminals electrically connected to the scan lines at one edge of the substrate, and the step of patterning the metal layer and the transparent conductive layer further comprises forming a plurality of second terminals electrically connected to the data lines at another edge of the substrate.

[c4] 4. The method of fabricating the thin film transistor array substrate of claim 3, further comprising forming a plurality of first transparent conductive layers on the gates, the scan lines and the first terminals.

[c5] 5. The method of fabricating the thin film transistor array substrate of claim 3, wherein the step of forming the passivation layer comprises exposing the metal layers on the pixel regions and the second terminals, and the step of removing the metal layers exposed by the passivation layer includes exposing the transparent conductive lay-

ers on the pixel regions and the second terminals.

[c6] 6. The method of fabricating the thin film transistor array substrate of claim 1, wherein the step of forming the gates and the scan lines further comprises forming a common lines, wherein the common lines serve as bottom electrodes of a plurality of pixel capacitors and the pixel electrodes above the common lines serve as plate electrodes of the pixel capacitors.

[c7] 7. The method of fabricating the thin film transistor array substrate of claim 1, further comprising forming a plurality of first transparent conductive layers on the gates, the scan lines and the common lines.

[c8] 8. A method of fabricating a thin film transistor array substrate, comprising:
forming a plurality of gates, a plurality of scan lines and a plurality of first terminals on a substrate, wherein the scan lines electrically connected to the gates and the first terminals;
forming a gate insulating layer covering the gates, the scan lines and the first terminals;
forming a channel material layer on the gate insulating layer;
forming a photoresist layer over the substrate, wherein the photoresist layer exposes the channel material layers

on the first terminals, and a thickness of the photoresist layer corresponding to the gates is thicker than a thickness of the photoresist layer corresponding to others;

removing the channel material layer and the underlying gate insulating layer exposed by the photoresist layer to expose the first terminals;

removing a plurality of portion of the photoresist layer until the channel material layer is exposed except that above the gates to remain a remained photoresist layer above the gates;

patterning the channel material layer using the remained photoresist layer as a mask layer to define and form a plurality of channel layers on the gate insulating layer formed above the gates;

forming a transparent conductive layer over the substrate;

forming a metal layer on the transparent conductive layer;

patterning the metal layer and the transparent conductive layer to form a plurality of source/drain regions, a plurality of data lines, a plurality of pixel regions, a plurality of second terminals and a plurality of conductive clumps, wherein the conductive clumps are on the first terminals and electrically connect to the second terminals, and the data lines electrically connect to the source/drain regions and the second terminals;

forming a passivation layer over the substrate exposing the metal layer on the pixel regions, the second terminals and the conductive clumps; and
removing the metal layer exposed by the passivation layer to expose the transparent conductive layer on the pixel regions, the second terminals and the conductive clumps, using the passivation layer as a mask, wherein the transparent conductive layer on the pixel regions serves as a plurality of pixel electrodes.

[c9] 9. The method of fabricating the thin film transistor array substrate of claim 8, further comprising forming a wherein the transparent conductive layer on the pixel regions serves as a plurality of pixel electrodes of first transparent conductive layer on the gates, the scan lines, the first terminals and the second terminals.

[c10] 10. The method of fabricating the thin film transistor array substrate of claim 8, wherein the step of forming the gates, the scan lines and the first terminals further comprises forming a plurality of common line, and wherein the common lines serve as bottom electrodes of a plurality of pixel capacitors and the pixel electrodes above the common lines serve as a plurality of plate electrodes of the pixel capacitors.

[c11] 11. The method of fabricating the thin film transistor ar-

ray substrate of claim 10, further comprising forming a plurality of first transparent conductive layers on the gates, the scan lines, the first terminals and the common lines.

[c12] 12. The method of fabricating the thin film transistor array substrate of claim 8, further comprising forming an ohmic contact layer on the channel layer before the step of forming a photoresist layer over the substrate is performed.

[c13] 13. The method of fabricating the thin film transistor array substrate of claim 8, wherein a material of the photoresist layer is positive photoresist, and the step of forming the photoresist layer on the channel material layer includes using a photomask, the photomask has a plurality of transparent areas corresponding to a plurality of position of the first terminals, a plurality of opaque areas corresponding to a plurality of positions of the gates and a plurality of semi-opaque areas corresponding to a plurality of positions rather than the first terminals and the gates.

[c14] 14. The method of fabricating the thin film transistor array substrate of claim 8, wherein a material of the photoresist layer is negative photoresist, and the step of forming the photoresist layer on the channel material

layer includes using a photomask, the photomask has a plurality of opaque areas corresponding to a plurality of positions of the first terminals, a plurality of transparent areas corresponding to a plurality of positions of the gates and a plurality of semi-opaque areas corresponding to a plurality of positions rather than the first terminals and the gates.

[c15] 15. The method of fabricating the thin film transistor array substrate of claim 8, wherein the step of removing the portion of the photoresist layer except that above the gates includes using an ashing process.